



|  |           |   |                          |
|--|-----------|---|--------------------------|
| INFORMATION DISCLOSURE CITATION<br>PAGE 1 OF 1                         |           | Atty Docket No.<br>TRA-078  | Serial No.<br>10/647,018 |
|  |           | Applicant<br>Zahi Abuhamdeh et al.  |                          |
|  |           | Filed<br>August 22, 2003  | Group                    |
| OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, Etc.) |           |   |                          |
| 2/10/06  | DG        | "SCANSTA 101 Low Voltage IEEE 1149.1 STA Master", Specification Rev. DS101215, National Semiconductor Inc.; October, 2002                     |                          |
| 2/10/06  | DG        | "IEEE Std. 1149.1 (JTAG) TAP Masters with 8-BIT Generic Host Interfaces" Embedded Test-Bus Controllers; SCBS676D-December 1996-Revised 8/2002 |                          |
| 2/10/06  | DG        | "IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices", ALTERA September 2000, ver. 4.05 ; Application Note 39                          |                          |
| 2/10/06  | DG        | "A Brief Introduction to the JTAG Boundary Scan Interface", Nick Patavalis, Athens; November 8, 2001  |                          |
|  |           |   |                          |
|  |           |   |                          |
|  |           |   |                          |
|  |           |   |                          |
|  |           |   |                          |
|  |           |   |                          |
|  |           |   |                          |
|  |           |   |                          |
|  |           |   |                          |
|  |           |   |                          |
|  |           |   |                          |
| EXAMINER   | 2/8/andri |   | DATE CONSIDERED 2/10/06  |